IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Inventor(s):
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Title: Microprocessor Including a Mode Detector for Setting Compression Mode

CERTIFICATE OF EXPRESS MAIL
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PRELIMINARY AMENDMENT

Commissioner for Patents
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Sir:

Prior to examining the above-identified application, please enter the following amendment:

IN THE CLAIMS:

Please delete Claims 1 – 41.

Please add the following claims.

--42. A method for executing a program including a first routine and a second routine in a microprocessor, comprising:

executing a branch instruction within said first routine, wherein said branch instruction indicates that said second routine is to be executed via a target address of said branch instruction; and

examining an indication specified by said branch instruction, wherein said second routine is determined to be coded using compressed instructions if said indication is in a first state, and wherein said second routine is determined to be coded using non-compressed instructions if said indication is in a second state different than said first state.

43. The method as recited in claim 42 wherein said branch instruction is a call instruction, wherein said executing includes storing a return address.

44. The method as recited in either claim 42 wherein said indication comprises a bit and said first state comprises said bit being set.

45. The method as recited in claim 44 wherein said second state comprises said bit being clear.

46. The method as recited in claim 42 further comprising storing said indication in a program counter within said microprocessor.

47. The method as recited in claim 42 wherein said indication serves as a compression mode for said second routine.

48. The method as recited in claim 47 further comprising decompressing instructions from said second routine if said compression mode indicates compressed.

49. The method as recited in claim 43 further comprising executing a return instruction at completion of said second routine, wherein said return instruction indicates said return address.

50. The method as recited in claim 49 further comprising examining a second bit within said return address, wherein said first routine is determined to be coded using compressed instructions if said second bit is in a first state, and wherein said first routine is determined to be coded using non-compressed instructions if said second bit is in a second state different than said first state.

51. An apparatus for executing a program including a first routine and a second routine in a microprocessor, comprising:

an executing means for executing a branch instruction within said first routine, wherein said branch instruction indicates that said second routine is to be executed via a target address of said branch instruction; and

an examining means for examining an indication specified by said branch instruction, wherein said examining means determines that said second routine is coded using compressed instructions if said indication is in a first state, and wherein said examining means determines that said second routine is coded using non-compressed instructions if said indication is in a second state different than said first state.

52. The apparatus as recited in claim 51 wherein said branch instruction is a call instruction, wherein the executing means is configured to store a return address in response to executing said call instruction.

53. A microprocessor, comprising:

a mode detector configured to detect a compression mode of a target routine in response to a branch instruction, wherein said branch instruction specifies an address and the compression mode of said target routine; and

an execution unit coupled to said mode detector, wherein said execution unit is configured to execute compressed instructions if said compression mode indicates compressed, and wherein said execution unit is configured to execute non-compressed instructions if said compression mode indicates non-compressed.

54. The microprocessor as recited in claim 53 wherein a particular bit specified by said branch instruction identifies said compression mode.

55. The microprocessor as recited in claim 54 wherein a particular bit within said branch instruction identifies said compression mode.

56. The microprocessor as recited in claim 53 further comprising a storage device coupled to the mode detector and configured to store a compression enable indicator, wherein the mode detector is configured to detect the compression mode responsive to the compression enable indicator.

57. A microprocessor adapted to operate on compressed instructions in addition to non-compressed instructions, wherein the microprocessor comprises:

a mode detector configured to receive a branch instruction specifying a compression mode indication, the mode detector configured to provide a compression mode signal in response to the compression mode indication of the branch instruction;

an execution unit configured to execute non-compressed instructions, wherein the execution unit is configured to update a current compression mode in response to the compression mode signal provided from the mode detector; and

an instruction decompressor coupled to provide non-compressed instructions to the execution unit, wherein the instruction decompressor is configured to selectively decompress received instructions into non-compressed instructions depending on the current compression mode.

58. The microprocessor as recited in claim 57 wherein said branch instruction is a call instruction, wherein the execution unit is configured to store a return address in response to executing said call instruction.

59. The microprocessor of claim 58, further comprising a return address register for storing said return address, wherein the return address register is configured to store the current compression mode when the execution unit executes the call instruction and to restore the current compression mode to the program counter upon execution of a subroutine return instruction.

60. The microprocessor of claim 58, wherein said compression mode indication is a least significant bit of a target address.

61. A method for executing a program including a first routine and a second routine in a microprocessor, comprising:

executing a branch instruction within said first routine, wherein said branch instruction indicates that said second routine is to be executed via a target address of said branch instruction, and wherein an operand of the branch instruction includes an indication; and

examining the indication, wherein said second routine is determined to be coded using compressed instructions if said indication is in a first state, and wherein said second routine is determined to be coded using non-compressed instructions if said indication is in a second state different than said first state.

62. The method as recited in claim 61 wherein said operand is an immediate operand.

63. The method as recited in claim 61 further comprising selectively decompressing instructions within said second routine responsive to said indication.

64. The method as recited in claim 61 further comprising updating a current compression mode responsive to the indication.

65. The method as recited in claim 61 wherein the branch instruction is a call instruction, and wherein the executing includes storing a return address.

66. The method as recited in claim 65 further comprising executing a return instruction within said second routine, the return instruction indicating the return address.

67. An apparatus comprising:

an executing means for executing a branch instruction within said first routine, wherein said branch instruction indicates that said second routine is to be executed via a target address of said branch instruction, and wherein an operand of the branch instruction includes an indication; and

an examining means for examining the indication, wherein said second routine is determined to be coded using compressed instructions if said indication is in a

first state, and wherein said second routine is determined to be coded using non-compressed instructions if said indication is in a second state different than said first state.

68. The apparatus as recited in claim 67 wherein said operand is an immediate operand.

69. The apparatus as recited in claim 67 further comprising a decompressing means for selectively decompressing instructions within said second routine responsive to said indication.

70. The apparatus as recited in claim 67 further comprising an updating means for updating a current compression mode responsive to the indication.

71. The apparatus as recited in claim 67 wherein the branch instruction is a call instruction, and wherein the executing means is configured to store a return address in response to executing the call instruction.

72. The apparatus as recited in claim 71 wherein the executing means is further configured to execute a return instruction within said second routine, the return instruction indicating the return address.

73. A microprocessor comprising:

a mode detector configured to detect a compression mode of a target routine in response to a branch instruction, wherein an operand of said branch instruction includes the compression mode of said target routine; and

an execution unit coupled to said mode detector, wherein said execution unit is configured to execute compressed instructions if said compression mode indicates compressed, and wherein said execution unit is configured to execute non-compressed instructions if said compression mode indicates non-compressed.

74. The microprocessor as recited in claim 73 wherein said operand is an immediate operand.

75. The microprocessor as recited in claim 73 further comprising an instruction decompressor within the execution unit, the instruction decompressor configured to selectively decompress instructions within said second routine into non-compressed instructions responsive to said indication.

76. The microprocessor as recited in claim 73 wherein the branch instruction is a call instruction, and wherein the execution unit is configured to store a return address in response to executing the call instruction.

77. The microprocessor as recited in claim 76 wherein the execution unit is further configured to execute a return instruction within said second routine, the return instruction indicating the return address.

78. A microprocessor adapted to operate on compressed instructions in addition to non-compressed instructions, wherein the microprocessor comprises:

a mode detector configured to receive a branch instruction having an operand including a compression mode indication, the mode detector configured to detect a compression mode in response to the compression mode indication of the branch instruction;

an execution unit configured to execute non-compressed instructions, wherein the execution unit is configured to update a current compression mode in response to the compression mode detected by the mode detector; and

an instruction decompressor coupled to provide non-compressed instructions to the execution unit, wherein the instruction decompressor is configured to selectively decompress received instructions into non-compressed instructions depending on the current compression mode.

79. The microprocessor as recited in claim 78 wherein said operand is an immediate operand.

80. The microprocessor as recited in claim 78 wherein the branch instruction is a call instruction, and wherein the execution unit is configured to store a return address in response to executing the call instruction. --

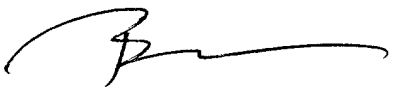
81. The microprocessor as recited in claim 78 wherein the execution unit is further configured to execute a return instruction within said second routine, the return instruction indicating the return address.

REMARKS

Claims 1 - 41 are pending in the application. Claims 1 - 41 have been cancelled. Claims 42 - 81 have been added. Claims 42 – 81 accordingly remain pending in the application.

A Fee Authorization form is enclosed; however, the Commissioner is hereby authorized to charge any additional fees which may be required to Deposit Account No. 12-2252/5201-02906/P2920-1D/BNK.

Respectfully submitted,



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